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Review

A Review on Fundamentals of Noise-Shaping SAR ADCs and Design Considerations

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Abstract: A general overview of Noise-Shaping Successive Approximation Register (SAR) analog-to-digital converters is provided, encompassing the fundamentals, operational principles, and key architectures of Noise-Shaping SAR (NS SAR). Key challenges, including inherent errors in processing circuits, are examined, along with current advancements in architecture design. Various issues, such as loop filter optimization, implementation methods, and DAC network element mismatches, are explored, along with considerations for voltage converter performance. The design of dynamic comparators is examined, highlighting their critical role in the SAR ADC architecture. Various architectures of dynamic comparators are extensively explored, including optimization techniques, performance considerations, and emerging trends. Finally, emerging trends and future challenges in the field are discussed.

Keywords: analog–digital conversion; noise shaping; SAR; oversampling; mismatch; comparator

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1. Introduction

The 21st century has pushed the capabilities of any analog-to-digital converter (ADC) to the limit, caused by the growing demand for various applications in low-power devices and the need to extend the life of batteries [1–3]. In practice, both the applications and their respective requirements are an open problem because current developments are powered with low voltages (<1.1 V). The challenge is to design architectures that are tolerant to the effect of these and other sources of error. Up to date, various types of ADCs have been implemented to push their performance to the limit and meet the requirements that each application demands; outstanding is the search for low power consumption and the number of bits that impacts the signal-to-noise and distortion ratio (SNDR) and the oversampling ratio (OSR), among other characteristics. It is important to note that many of these metrics are correlated; Figure 1 illustrates the main ADC architectures in terms of their bandwidth and resolution [4–8].

For certain applications, preserving the minimum power consumption is a crucial key, and SAR is the best exponent due to the reduced hardware used in its construction, a characteristic that can be seen in Figure 2, where the power consumption against the sampling frequency, fs, in SAR, NS SAR, and Sigma Delta ($\Sigma\Delta$) implementations, which are continuous-time (CT) and switched-capacitor (SC) [9], is shown. SAR has demonstrated an adequate balance in power consumption, moderate bit resolution (≈14 bits), and SNDR. However, many implementations have been limited to 80 dBs of SNDR. To increase this metric, the quantization error feedback is used in combination with the oversampling technique to apply "noise shaping" in the SAR, always keeping a low power consumption. This quality has made the NS SAR an attractive option for its integration in system-on-chip (SoC) interfaces and its manufacturing feasibility in nanometric CMOS technologies, where efforts have been focused on improving the BW [10]. In practice, NS SAR is not an ideal

converter. At the circuit level, there are a series of implications that affect the linearity of the converter, which impacts the overall performance of the ADC. These drawbacks have led to a redesign of SAR A/D conversion, and this explains why new proposals have replaced continuous consumption circuits with switched proposals. In this way, sources that introduce nonlinearities into the conversion process are also eliminated and limited to using at least one active system, the voltage comparator, whose performance is purely dynamic. Today, optimizing the performance of the comparator is an open problem, and it seeks to increase its performance without incorporating static consumption circuits.

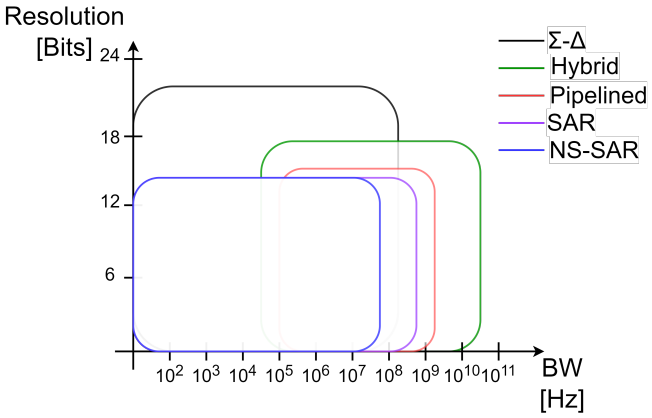

Figure 1. Types of ADCs comparative in terms of BW and resolution.

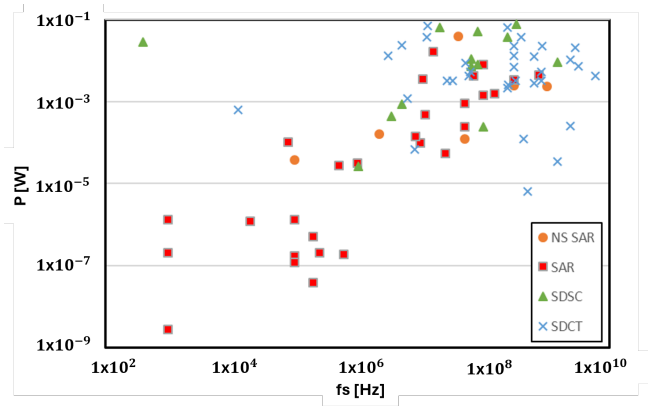

Figure 2. Power consumption comparison in conventional A/D converter architectures and in NS-SARs.

This document is divided into four sections. Section 2 presents the fundamentals of NS SAR ADC. Section 3 presents the main non-idealities of the NS SAR ADC, the problems and challenges to overcome. Relevant proposals that have recently added to the design of the dynamic comparator are described in Section 4, where their advantages/disadvantages are analyzed. Finally, Section 5 presents both the conclusions of this work and trends in NS-SAR A/D conversion.

2. From SAR ADC to NS SAR: Fundamentals

Understanding the operation of NS SAR is easier by starting with the analysis of a traditional SAR ADC structure shown in Figure 3. The A/D conversion system is based on a binary search algorithm, and with each conversion cycle it gets closer to the input value. The DAC is usually built with capacitive networks (CDAC) for its ease of scaling and its simple construction. The single-ended format for a 4-bit CDAC is shown in Figure 4; the operating principle is based on charge distribution and the generation of weighted voltages. The system includes two phases: sampling and conversion. The first phase captures the value of V_{in}, and all capacitors are connected by S_1, such that one plate of the capacitor is

connected to Vin and the other to GND. In the conversion stage, because the process starts with the N-bit midscale, the voltage at the inverting terminal of the comparator, V_x, will be determined by Equation (1); a representation of the capacitive voltage divider in the first cycle can be seen in Figure 5.

$$V_x = -V_{in} + d_{N-1}\frac{V_{ref}}{2} + d_{N-2}\frac{V_{ref}}{4} + \cdots + d_0\frac{V_{ref}}{2^N}, \quad (1)$$

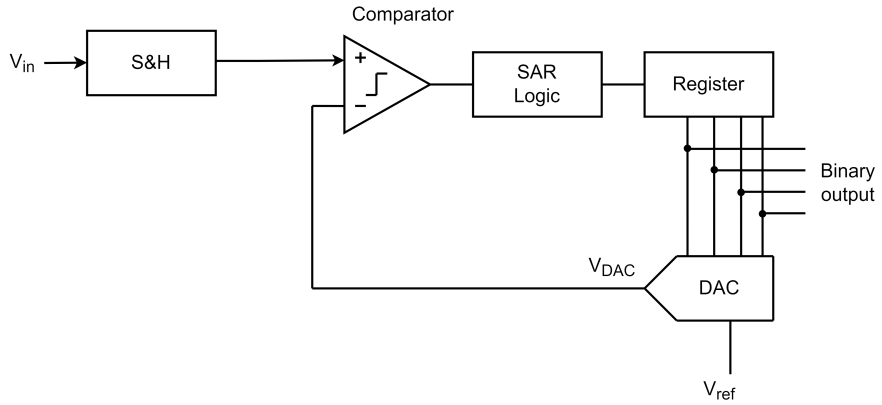

Figure 3. Traditional SAR ADC schematics.

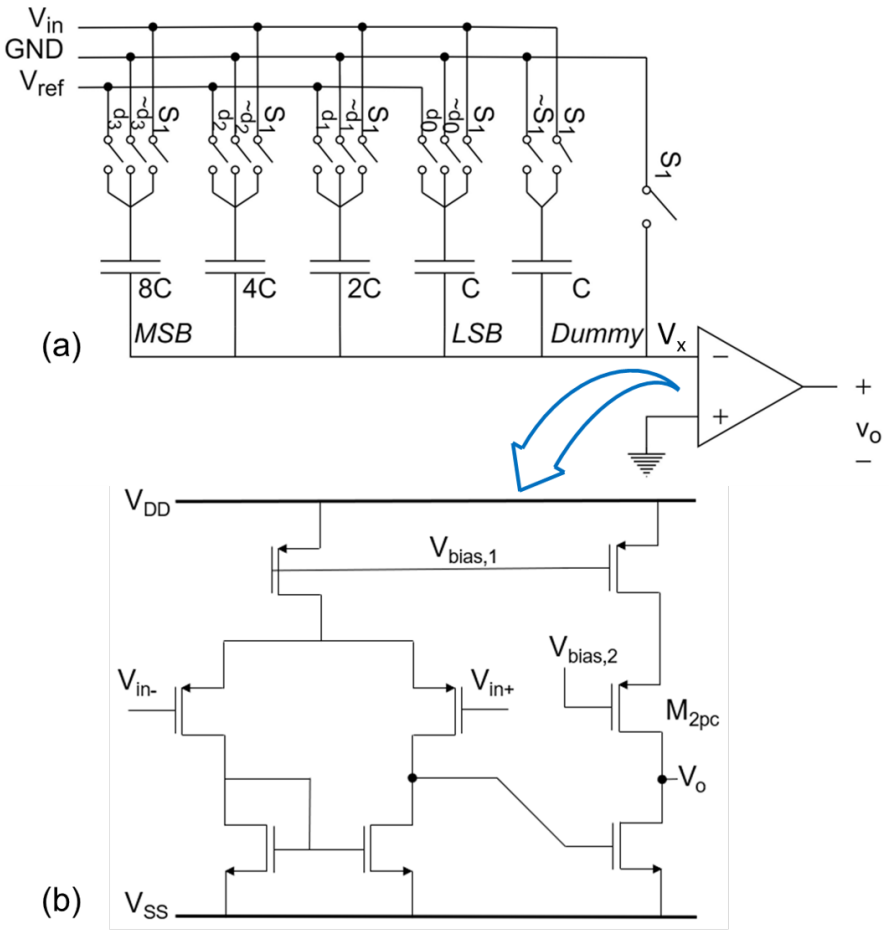

Figure 4. A 4-bit single-ended CDAC (**a**) and conventional comparator (**b**).

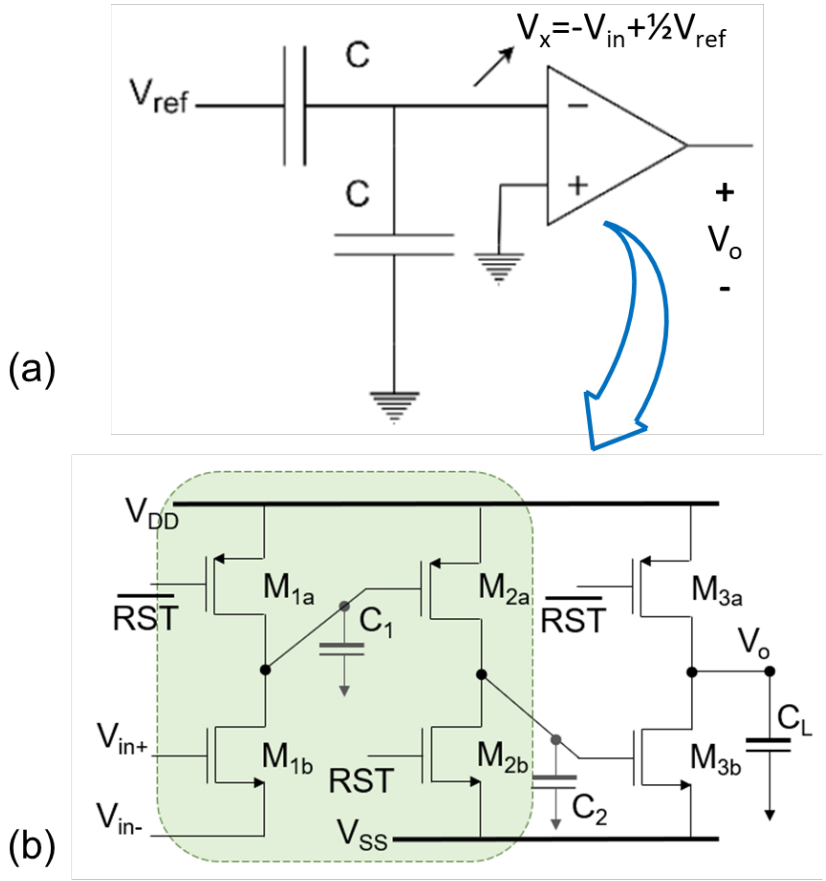

Figure 5. Capacitive voltage divider in the first conversion cycle (**a**) and comparator-based switched amplifier (**b**).

Note that this result assumes that the comparator is not only ideal, but that the weighted sum is not affected by the switching frequency, i.e., it is a noiseless analysis. It is important to note that the comparator is designed according to the characteristics of the ADC and the CDAC. Figures 4b and 5b show two types of single-output comparators. The first is a comparator implemented with a conventional differential amplifier, and the second is a comparator based on a switched amplifier. These comparators will be explained in detail in Section 4. Regardless of the sampling topology (bottom plate (a) or top plate (b), see Figure 6), at present the CDAC implementations are fully differential, because they benefit not only from noise rejection in the common mode, but also an improvement in the signal voltage range can be seen. The differential input signals can be defined as in Equations (2) and (3), where x is an arbitrary voltage; the voltage reference is "split", as per what is shown in Equations (4) and (5).

$$V_{inp} = x, \tag{2}$$

$$V_{inn} = V_{ref} - x, \tag{3}$$

$$V_{refp} = V_{CM} + \frac{V_{ref}}{2}, \tag{4}$$

$$V_{refn} = V_{CM} - \frac{V_{ref}}{2}, \tag{5}$$

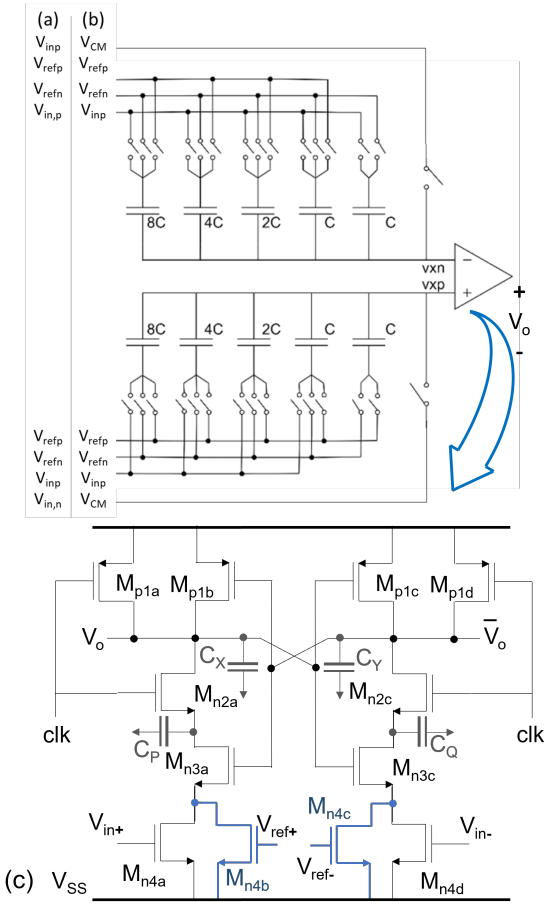

Figure 6. Four-bit CDAC sampling (**a**) top plate, (**b**) bottom plate, and (**c**) dynamic comparator.

The principle of operation of a fully differential structure is similar to the single-ended version, but now an identical capacitive network is added in the non-inverting terminal to process the "negative" signal. After the sampling phase (in both networks), the conversion cycles start at the midscale of the N bits. For example, in the 4-bit scheme shown in Figure 6b, the top network will have the 8C capacitor connected to Vrefp, and the other capacitors connected to V_{refn}, i.e., the digital word 10000, while the bottom network will always have the complement, in this case, the digital word 01111. Thus, the voltages on the comparator are determined by Equations (6) and (7). The comparator evaluates if $V_{xn} < V_{xp}$, if true, then the output will be a logical '1', otherwise it will be a logical '0'. Now, depending on the result of that comparison, a new digital word value will be evaluated in the next cycle. Suppose the comparison result was '1', so now in the next evaluation it will be 11000 for the upper network and 00111 for the lower network. Thus, capacitive networks modify their voltage divider and now the voltages will model Equations (8) and (9) at the input of the comparator; this process is repeated N times. A complete scheme of the 4-bit fully differential binary search algorithm can be seen in Figure 7. Once the conversion process is finished, A/D conversion is completed. However, the accuracy of the conversion is determined by the quantization process (and resolution), and since this is a non-linear process, a residual voltage remains due to the difference between the sampled input and the digital conversion estimate (in analog format). At the end of the conversion there will be a difference, or quantization error, <1 LSB. An open problem is to further reduce that value, so that the conversion increases its degree of linearity.

$$V_{xn} = -V_{inp} + V_{CM} + \frac{1}{2}V_{DD}, \tag{6}$$

$$V_{xp} = -V_{inn} + V_{CM} + \frac{1}{2}V_{DD}, \tag{7}$$

$$V_{xn} = -V_{inp} + V_{CM} + \frac{3}{4}V_{DD}, \tag{8}$$

$$V_{xp} = -V_{inn} + V_{CM} + \frac{1}{4}V_{DD}, \tag{9}$$

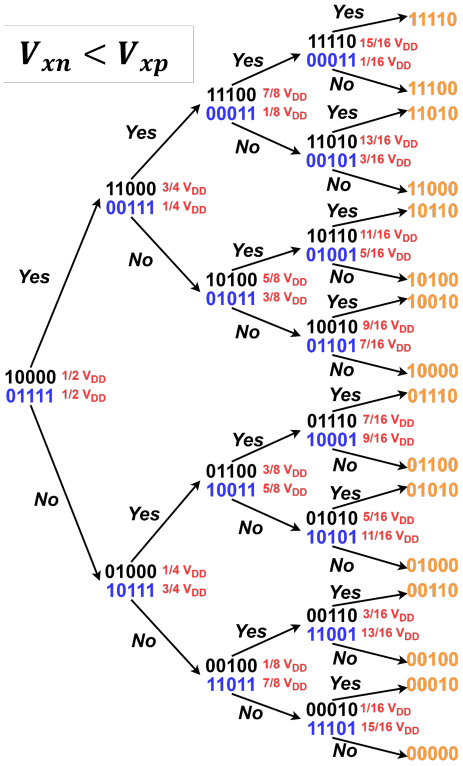

Figure 7. Full differential binary search algorithm in 4-bit CDAC.

Figure 8 illustrates the comparison voltages at each cycle of a 10-bit SAR ADC. With the natural progression in the conversion process, the voltages get closer to V_{CM}, and eventually, in one extra cycle, the quantization error can be processed in differential format.

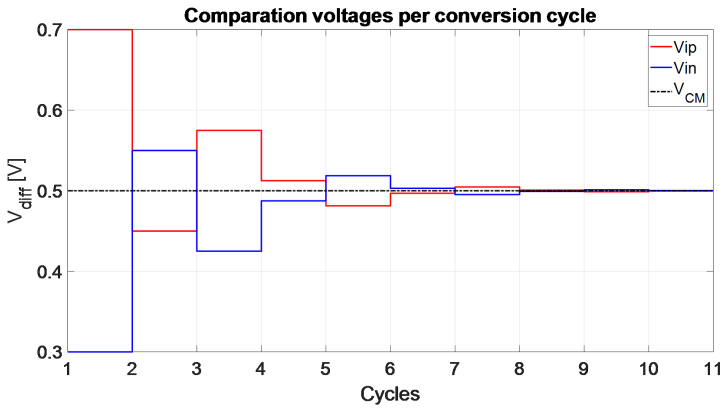

Figure 8. Differential conversion process of a 10-bit SAR ADC.

The experienced reader will be able to evoke what happens analogously in a ΔΣ modulator, where the main feature lies in oversampling and error feedback, to apply noise shaping to the quantization noise.

The distinctive feature of a NS SAR is the sampling and processing of the CDAC residual voltage (quantization error) and applying the noise-shaping technique using a filter. The technique distributes not only the quantization noise outside the BW of interest, but also shapes the comparator noise. This residue, or quantization error, is added to the conversion line to perform a noise shaping, where the synthesis of the various architectures has preference to those that include low consumption. A NS SAR consists of a SAR structure, a feedback filter for residual voltage processing, and a summation point for adding the quantization error to the conversion line. There are two main architectures for loop filter implementation and residual processing: Error Feedback (EF) and Cascade Integrator Feed-Forward (CIFF) [11,12], illustrated in Figure 9 and Figure 10, respectively.

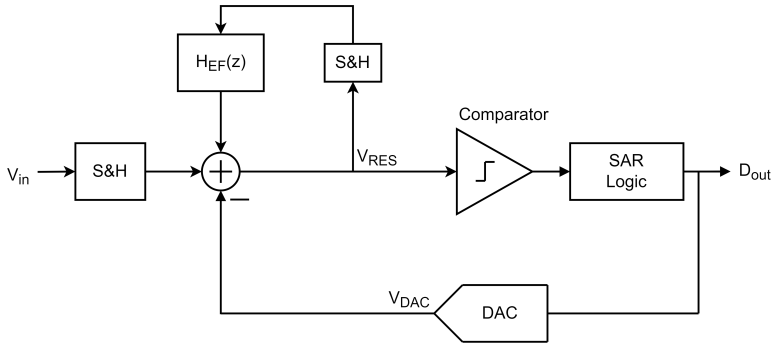

Figure 9. Error Feedback NS SAR schematics.

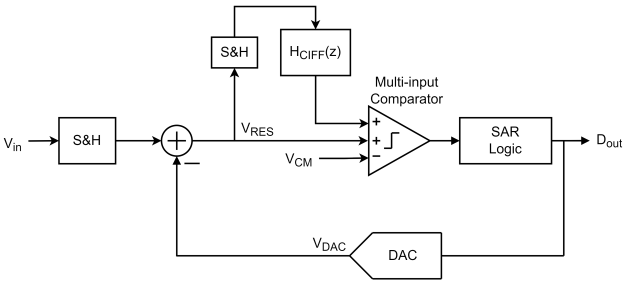

Figure 10. Cascade Integrator Feed-Forward NS SAR schematics.

2.1. Noise-Shaping SAR ADC Implementations: Error-Feedback and Cascade Integrator Feed-Forward

The block diagram of EF and CIFF structures are presented in Figures 11 and 12, respectively. Signal and noise transfer function analysis can be deduced from these diagrams, obtaining (10) and (11) for EF and CIFF, respectively. The noise transfer function NTF(z) can be identified as the factor that multiplies the quantization error E_Q(z), being $(1 - H_{EF}(z)z^{-1})$ for EF and $(1 + H_{CIFF}(z)z^{-1})^{-1}$ for CIFF.

$$D_{out}(z) = V_{in}(z) + E_Q(z)(1 - H_{EF}(z)z^{-1}), \tag{10}$$

$$D_{out}(z) = V_{in}(z) + E_Q(z)\left(\frac{1}{1 + H_{CIFF}(z)z^{-1}}\right), \tag{11}$$

EF implementations require a summing point to add the sampled signal and the quantization error, and the synthesis of this block determines the efficiency of the NTF [11]. The loop filter implementation can be active or passive [13]. Some recent reports [14,15] have incorporated a unity gain buffer instead of passive sampling to achieve lossless NTF. In these works, the use of ping-pong schemes for switching is adopted, which facilitates

fully passive implementations. Table 1 presents a comparison of important reported EF implementations.

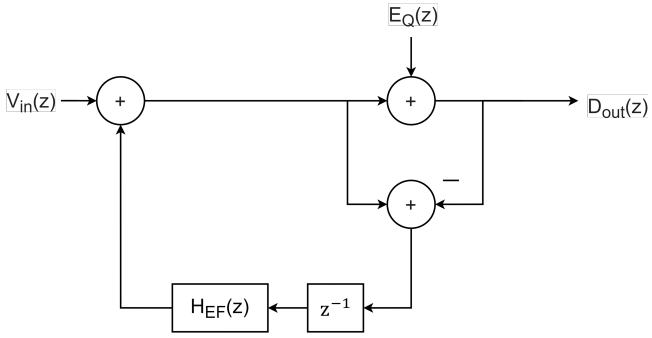

Figure 11. EF NS SAR ADC block diagram.

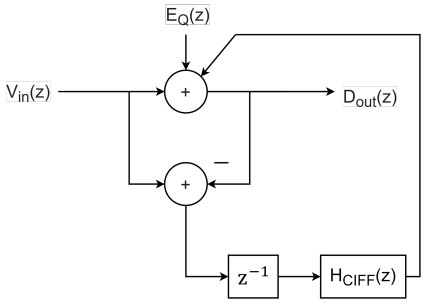

Figure 12. CIFF NS SAR ADC block diagram.

The latter metric allows for a punctual and "fair" comparison between the performance of the ADCs. This is the Figure of Merit (FoM) and it represents a relationship between resolution, conversion speed, and power consumption. There are two main FoMs for ADCs, Walden's FoM_W (12) and Schreier's FoM_S (13). The units of the first are J/conv-step and of the second, decibels. A lower FoM value indicates a lower value in power consumption with the same noise performance, which also implies a lower overall power consumption [16].

$$FoM_W = \frac{P}{f_s 2^{ENOB}}, \tag{12}$$

Table 1. Comparative performance of EF implementations.

Specification	Chen 2015 [13]	Li 2018 [17]	Yi 2022 [14]
Filter	EF	EF	EF
Process	65 nm	40 nm	65 nm
Order	1	2	1
Supply	0.8 V	1.1 V	1.2 V
Bits	8	9	9
BW	6.25 MHz	625 kHz	625 kHz
OSR	4	8	16
SNDR	58.03 dB	79 dB	81 dB
Power	120.7 µW	84 µW	183.6 µW
FoMs	165.1 dB	178 dB	176.3 dB

$$FoM_S = SNDR + 10log\left(\frac{f_s/2}{P}\right), \tag{13}$$

It is important to note that the number of CIFF implementations is greater than EF. The first report of a NS SAR was a CIFF structure [18]. In practice, the filter implements FIR-IIR for residual voltage processing, since the IIR stage provides additional gain. Note that in a CIFF implementation, for the quantization noise in Equation (11) to have a high-pass characteristic as in EF, H_{CIFF}(z) multiplied by z^{-1} should have the nature of an integrator ($z^{-1}/(1-z^{-1})$). This answer is an ideal representation, but in practice this does not happen. An equation that better models losses is (14). With a large value of α, the zero of NTF(z) is located closer to the unit circle, as illustrated in Figure 13, which allow for a more defined noise-shaping effect. However, to achieve a higher value α, a precise charge transfer is required in the integrator [19], which is generally based on the use of high-gain and high-BW OTAs. This type of implementation opposes the original idea of a NS SAR, which is to have a low power consumption and be scalable in CMOS technologies.

$$NTF(z)_{H_{CIFF}} = \frac{1}{1+\frac{\alpha}{1-\alpha z^{-1}}z^{-1}} = 1-\alpha z^{-1}, \tag{14}$$

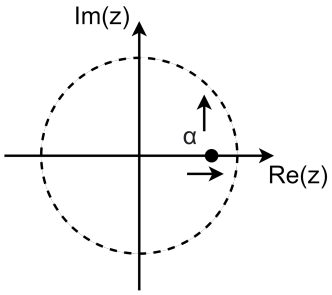

Figure 13. Representation of the value of α in a unit circle.

Concerning active implementations, those integrators with op-amps and switched capacitors (SC) stand out [18,20]. An active third-order approach proposed in [21] can be seen in Figure 14. That work is important because it uses duty cycling to reduce power consumption. In passive implementations, the issue is that there is no gain, and seeking to overcome this inconvenience, DA and capacitor stacking are the main architectures (Figures 15 and 16) since they offer low power consumption amplification [22,23]. However, DA gain is sensitive to PVT variations. Digital calibration is used to ensure PVT robustness, but it increases design complexity [24]. Implementations that include buffers [25] have also been used to deal with attenuation due to charge transfer. The source–follower topology is commonly used, but there are also modified versions such as the one described in [26]. Other works include a pre-amplifier, as mentioned in [27], but also pseudo-differential architectures of inverter-based circuits [28]. The scheme of a fully passive implementation is mentioned in [19]. Finally, it is important to point out that recent works incorporate the Closed-Loop DA [29] and the Ring Amplifier [30] as promising structures due to their robustness.

It is well known that the implementation of higher orders in the EF NTF(z) (greater than 2) is complicated because the FIR filter coefficients increase in quantity and are more sensitive to variation. For this reason, nested–cascade architectures have been proposed [31]. Hybrid third-order implementations combining EF and CIFF have also been reported [32,33], where both feedback and feed-forward addition are included. Because of the flexibility in the implementation of the IIR filter, recent resonators, CRFF (Cascade Resonator Feed-Forward), have been proposed [34], but also one that includes the resonator in a hybrid architecture (active–passive), achieving an improvement in BW [35]. A comparison of the cascaded implementations can be seen in Table 2.

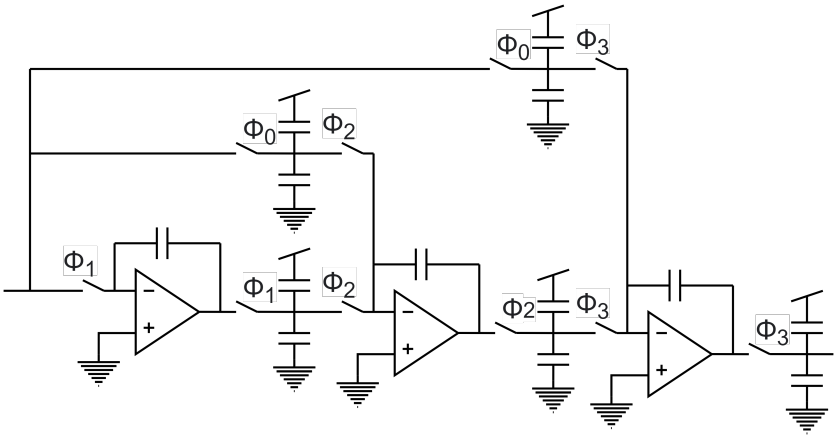

Figure 14. Active SC third-order implementation [21].

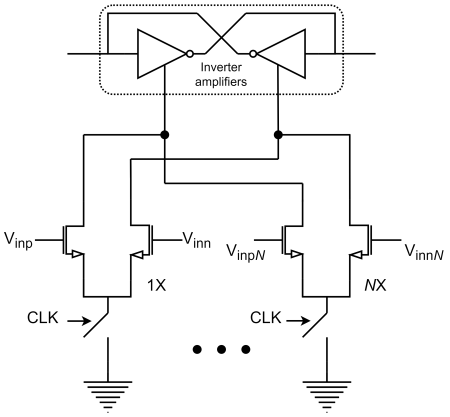

Figure 15. DA-based multi-input comparator.

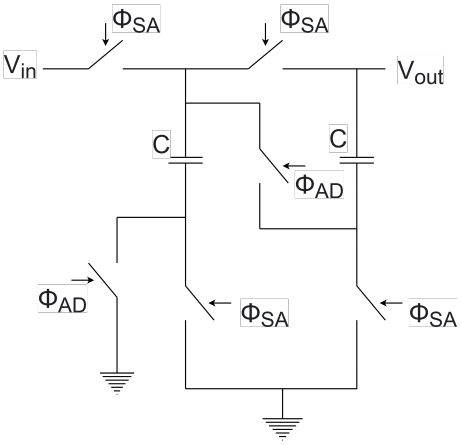

Figure 16. Capacitor stacking to double voltage.

Table 2. Comparative performance of cascaded/hybrid implementations.

Specification	Lu 2020 [31]	Wang 2021 [32]	Zhang 2022 [33]	Wang 2022 [34]	Fu 2022 [35]
Filter	Cascade-EF	EF-CIFF	EF-CIFF	EF-CRFF	CRFF
Process	28 nm	65 nm	130 nm	65 nm	180 nm
Order	4	3	3	4	2
Supply	1 V	1.1 V	1.2 V	2 V	1.8 V

Table 2. *Cont.*

Specification	Lu 2020 [31]	Wang 2021 [32]	Zhang 2022 [33]	Wang 2022 [34]	Fu 2022 [35]
Bits	10	10	8	10	10
BW	100 kHz	625 kHz	125 kHz	500 kHz	1 MHz
OSR	10	8	8	5	-
SNDR	87.6 dB	84.8 dB	79.5 dB	84.1 dB	89.4 dB
Power	120 µW	119 µW	96 µW	134 µW	880 µW
FoMs	176.8 dB	182 dB	170.7 dB	182.4 dB	187.3

2.2. Noise-Shaping Plots

The benefit of oversampling is that noise outside the band of interest can be filtered out from all noise-generating sources. However, it is necessary to process the noise that falls inside the band. Combining oversampling and quantization error feedback, noise shaping is achieved, and the idea is to have a lower value of noise in the band of interest. As an illustrative case, consider a SAR ADC with a 10-bit core, fs = 100 MHz, amplitude = 0.45 V, offset = 0.5 V, and BW of 1 MHz simulated behaviorally in MATLAB-Simulink® [36]. The process for plotting the power spectral density consists of applying a window to the output data, obtaining the fast Fourier transform (FFT), and then plotting the resulting spectrum. Figure 17 shows the power spectral density with SNDR, SNR and ENOB metrics for a traditional SAR ADC (Nyquist). If an EF structure is adopted and the quantization error is fed back in addition to a delay to the input sampled signal, the first-order noise shaping, presented in Figures 18 and 19, is achieved. Do not forget that an OSR must be defined for noise shaping to make sense. For illustrative purposes, it has been set to 16, although common OSRs for NS SAR range from 4 to 8. From the aforementioned plots, it is important to note two features: the slope of the noise shaping (20 dB/decade), and within the BW of interest (1 MHz), the noise has a higher attenuation compared to the Nyquist SAR. Also note the increment in the values of the performance metrics, approximately 30 dB in SNDR and SNR and just over 5 bits in ENOB.

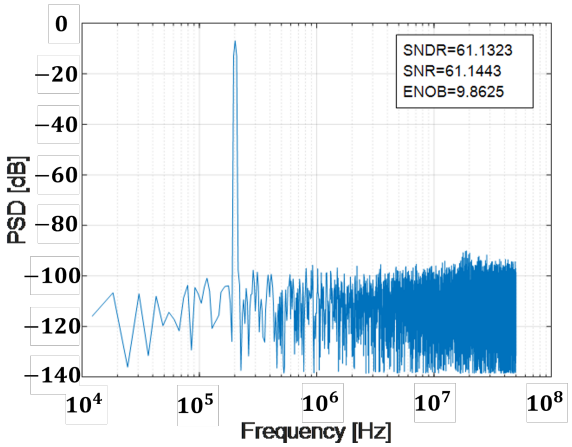

Figure 17. PSD without noise shaping.

But, how to get NTF(z) implementations of higher orders? Recalling Equation (10), it has been seen that if $H_{EF}(z)$ is equal to unity, and only the quantization error is fed back with a delay, a first-order shaping is achieved. Now, what should be the value of $H_{EF}(z)$, to have a second-order NTF(z), $(1 - z^{-1})^2$? If a filter that models $(2 - z^{-1})$ is implemented, as can be seen in Equation (15), NTF(z) will shape the quantization noise at a rate of 40 dB/decade, as shown in Figure 20. Similarly, to get a third-order NTF(z), $H_{EF}(z)$ must

be equal to $(3 - 3z^{-1} + z^{-2})$, as shown in Equation (16). Figure 21 presents the PSD plot for a third-order implementation.

$$NTF(z)_{2_{Or}} = 1 - (2 - z^{-1})z^{-1} = (1 - z^{-1})^2, \tag{15}$$

$$NTF(z)_{3_{Or}} = 1 - (3 - 3z^{-1} + z^{-2})z^{-1} = (1 - z^{-1})^3, \tag{16}$$

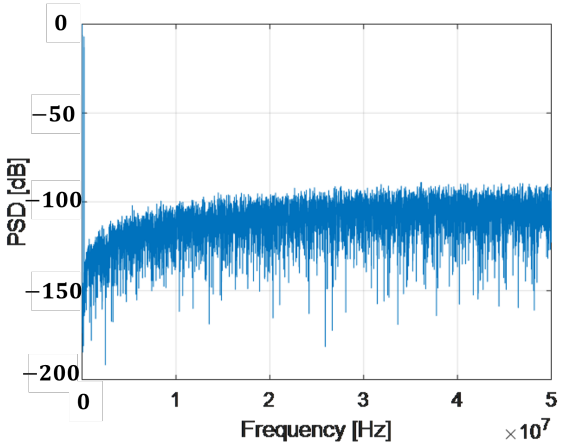

Figure 18. PSD with first-order noise shaping.

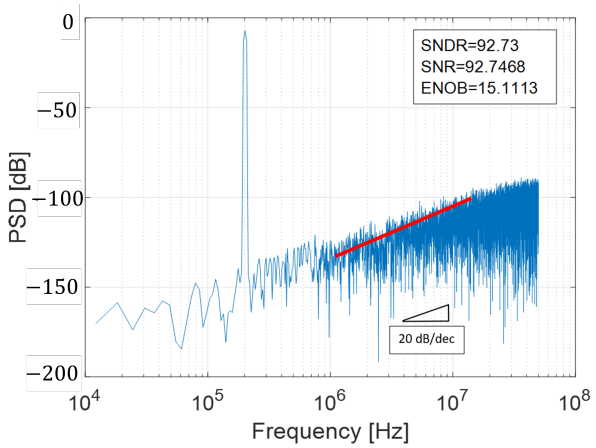

Figure 19. Semilog chart of PSD with first-order noise shaping and 20 dB/dec slope.

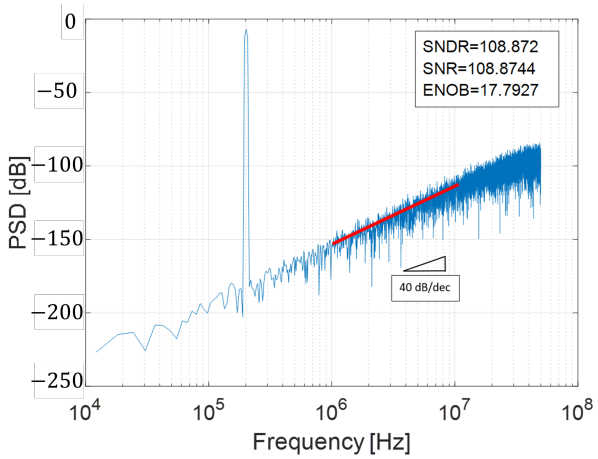

Figure 20. PSD with second-order noise shaping.

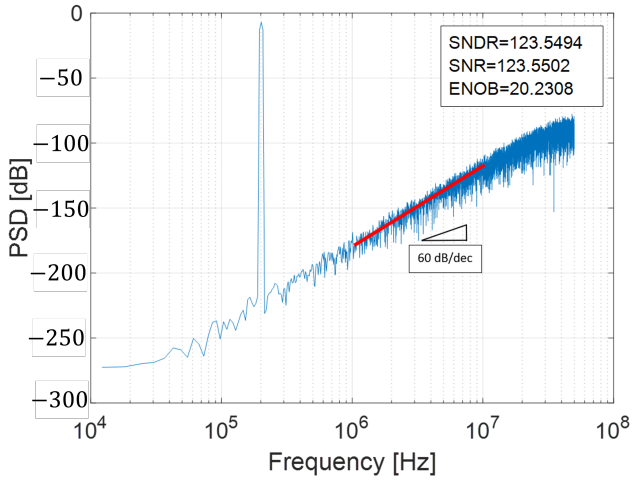

Figure 21. PSD with third-order noise shaping.

3. Non-Idealities in the Performance of NS SAR ADC: Problems, Challenges and Solutions

In practice, A/D conversion systems are oriented towards silicon synthesis. Beyond the challenges that the topologies themselves impose on the implementation (on the passive or active filters, on the comparator, etc.), it must be considered that the different sources of error add non-linearity to the converter.

Table 3 presents the main problems of NS SAR, as well as the solutions and techniques used to date. In general, it is known that the disadvantage of noise shaping is that all loop filters introduce thermal noise, which is not shaped. Regarding the implementations, it is necessary to mention that although the dynamic multi-input comparator has been a well-accepted technique, its disadvantage is that each input represents a noise source. But, the most important noise sources influencing the nonlinearity of the NS SAR ADC are CDAC mismatch, kT/C noise, flicker, and comparator offset.

3.1. Mismatch in CDAC

CDAC binary weighted capacitors are manufactured in two ways in MOS technologies: metal–insulator–metal (MIM) and metal–oxide–metal (MOM). Both are subject to variations in physical parameters (due to the manufacturing process) and are the cause of the error that contributes to the CDAC non-linearity. By not having exact capacitor values (and their weights), non-uniform conversion code widths are generated. This is because the unit capacitance is intended to be minimal to benefit power consumption. In contrast, as the technologies scale, the unit capacitances are of a smaller value, increasing the standard deviation. Therefore, the error also increases, becoming so severe that the conversion error (after calibration) can be greater than 1 LSB [37]. Illustratively, the non-linearity of the conversion process can be seen in Figure 22. The need to incorporate techniques that mitigate the impact and manage the effects of mismatch is evident. To appreciate the impact of the mismatch on the NS SAR, Figure 23 shows the PSD of the EF NS SAR presented in Figure 19, but with a CDAC capacitive mismatch of 1%. Note that the metrics have decreased from the performance shown in Figure 19, SNDR at about −9 dB and ENOB at −1.5 bits. SFDR is the ratio of the amplitude of the input signal to the amplitude of the largest spurious signal in the frequency range of interest. Ideally, a pure signal has the power concentrated at its fundamental frequency. However, due to the non-linearity of the components, there is an undesirable value of third harmonic distortion in fully differential architectures [1]. There are various techniques for correcting the mismatch (see Table 3). Although increasing the area of the capacitors solves the mismatch problem, it is not feasible because it is not scalable. Digital calibration (foreground and background) is a common technique; here, it is required to previously know an estimate of the error due to mismatch. LMS (Least Mean Squared) [17,37,38] is a digital calibration method that has

generated remarkable values of SFDR. This calibration method can be of the foreground or background type. Its operation is based on the fact that it obtains the exact weight of each capacitor in the CDAC network (from the conversion results) and corrects the errors with the calibrated weights. With digital techniques, values of up to 105 dB of SFDR have been achieved [39].

Table 3. Challenges and solutions in the design of NS SAR.

Problem	Solutions	Techniques
Mismatch in DAC	Increment in CDAC area	· Larger DAC unit elements
	Digital calibration	· Foreground · Background
	Digital Mismatch Shaping-Dynamic Element Matching (DEM)	· Data Weighted Averaging (DWA) · Segmented DEM
	Mismatch Error Shaping (MES)	· Preset of LSBs
kT/C and flicker noise + offset	Switches and amplifiers designs	· Clock Boosting · Bootstrapping · Buffer design · Chopper modulation

Mismatch Error Shaping (MES) has also been a good alternative. This is a total analog implementation and 105 dB of SFDR have been reported [40]. Its operating principle focuses on the fact that the mismatch error is fed back and conformed with a high-pass filter function, $(1-z^{-1})$. To achieve this, the key is to preset the CDAC LSBs in NS SAR before sampling, so that the mismatch error from previous conversions is captured during sampling, as shown in Figure 24. Note that the MSB is not fed back, i.e., GND is naturally conserved, since it is considered to be a precise reference. Then, the LSBs are reset and the natural conversion continues [20]. The general idea is that the preset LSBs from the previous conversion are subtracted from the current signal [12] and then a first-order shaping (17) is achieved. Also, redundancy LSBs can be added to correct the so-called DAC settling.

$$V_o(n) = V_{in}(n) + E(n) - E(n-1), \tag{17}$$

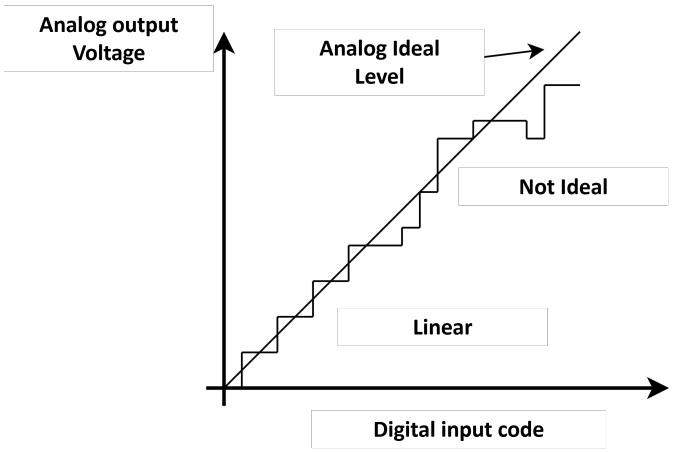

Figure 22. Linear and non-linear characteristics in A/D conversion.

A drawback of using MES is the overrange, produced by the extra voltage added to the input of the converter, which should not exceed the V_{LSB} limits of $-1/2V_{ref}$ and $+1/2V_{ref}$ [41]. Recent MES techniques have adopted a two or three-level predictive process to correct overrange and compensate for extra voltage. In the first-order MES works

reported in [16,41], values of 98 dB of SFDR have been obtained; it has also been demonstrated that a second-order shaping can be achieved, reaching values of SFDR as high as 122 dB [42]. Other alternatives such as the use of the double sampling technique [40] and pre-comparison [43] have reported values of 104.5 dB and 103 dB, respectively.

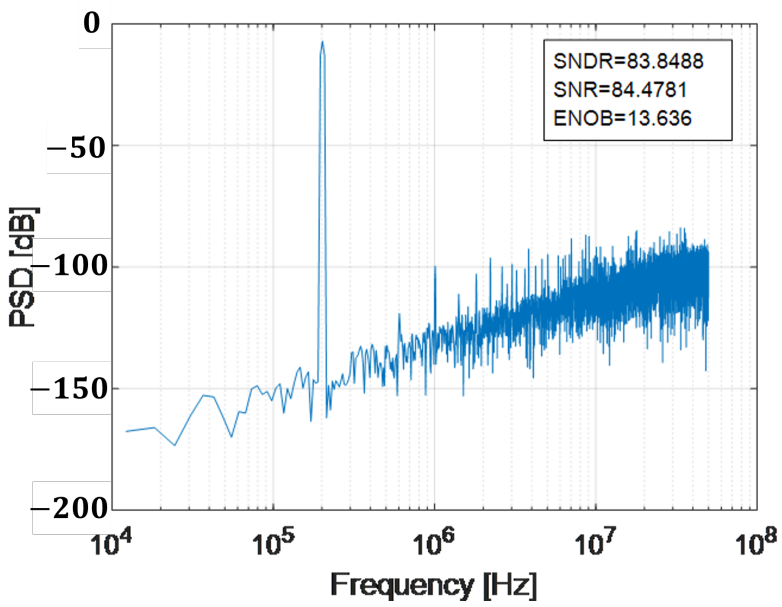

Figure 23. PSD with one mismatch in a first-order implementation EF.

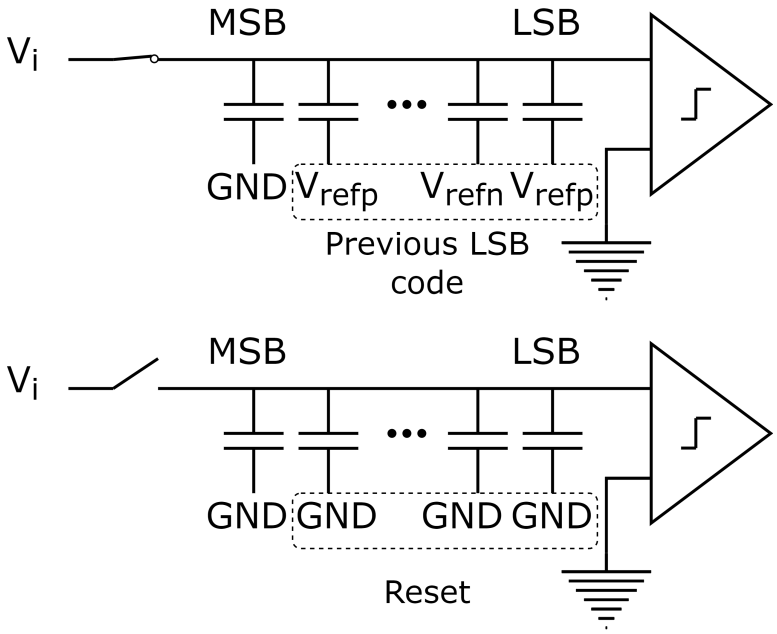

Figure 24. First-order MES. Sampling phase and LSBs reset stage.

An alternative for mismatch correction is Dynamic Element Matching (DEM), which uses algorithms to select unitary components and average the elements. Figure 25 illustrates the operation of the DEM, where the digital output signal is encoded on a thermometric scale, and with the implemented algorithm, the selection of unitary components is applied. Note that the implementation can be excessive as the number of bits increases. Data Weighted Averaging (DWA) is a remarkable algorithm, but there are also Butterfly Randomization, Individual Level Averaging, and Tree Structure techniques. For example, a combination of DEM and Dither [21] reported 112 dB of SFDR, where the disadvantage is a BW of 2 kHz.

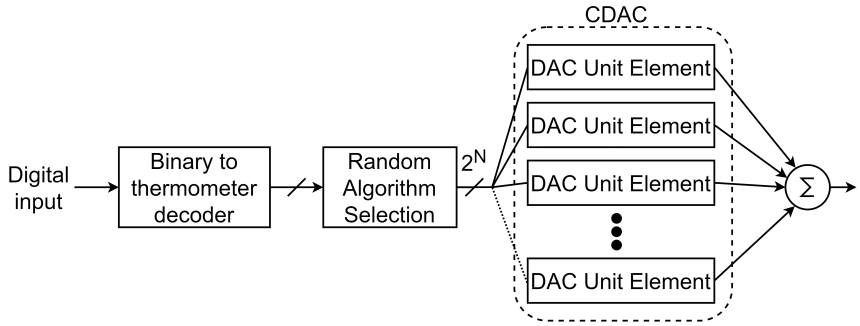

Figure 25. DEM process.

The operating principle of the DWA is based on the selection of elements in a rotating manner, so that the output value of the CDAC is the sum of the unit elements selected cyclically. The selection ensures that the mismatch error is averaged as fast as possible, in such a way that they are modulated with a high-pass filter function, $(1 - z^{-1})$, as described in Equation (18) [44]. Figure 26 presents an example of the DWA algorithm for a 3-bit DAC, which corresponds to eight unit elements. In each cycle the selection of the first element is made from the element that follows after the last selected element of the previous cycle (for example, in the first cycle the input code is 1, and in the second cycle it is 3, but three elements are selected from element 1, that is, from element 2 to 4), that is why the "pointer" is implemented, because in each new conversion cycle the pointer is updated, and it is necessary to know the value of the last selected element so that the current error is subtracted from the past error [45]. However, combinations of both techniques have been used, DWA for the most significant bits and MES for the least significant, and thus compensate the disadvantages of each one. The most significant works that incorporate this combination of techniques have reached outstanding values [20,23,46]. Table 4 summarizes the main implementations according to the technique used and the SFDR value achieved.

$$V_o(z) = V_{in}(z) + (1 - z^{-1})E(z), \tag{18}$$

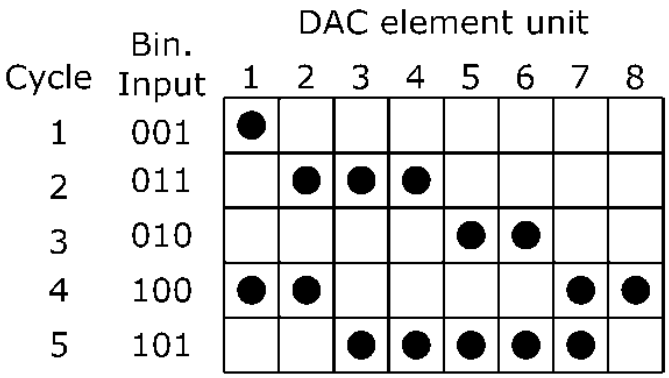

Figure 26. Unit element selection using DWA algorithm.

Table 4. Comparative mismatch correction techniques.

Reference	Calibration Technique	SFDR [dB]
Li 2018 [17]	Background LMS	89
Zhuang 2019 [24]	Background LMS	90
Jie 2020 [47]	LUT Foreground	102.8
Liu 2021 [39]	Foreground	104.4
Wang 2021 [32]	Foreground LMS	103

Table 4. *Cont.*

Reference	Calibration Technique	SFDR [dB]
Liu 2019 [42]	MES	122*
Yang 2022 [40]	MES	104.5
Li 2021 [41]	MES	98
Shen 2022 [43]	MES	103
Li 2022 [16]	MES	98
Obata 2016 [21]	DEM + Dither	112
Miyahara 2017 [48]	Binary mode DEM	84.3
CC Liu 2017 [49]	DWA	92.2
Zhang 2020 [50]	DWA	97.34
Zhang 2021 [27]	DWA	92.9
Shu 2016 [20]	MES + DWA	105.1
Liu 2020 [23]	MES + DWA	102.2
Hasebe 2022 [46]	MES + DWA	108.5

3.2. CDAC Mismatch Correction, an Alternative: NS DEM

The block diagram of the NS SAR with the different error sources is presented in Figure 27. E_S(z) is the sampling error (mostly kT/C noise); $E_Q(z)$ represents quantization errors, comparator noise, and DAC settling; $E_D(z)$ is the DAC mismatch error; and $E_{N1}(z)$ and $E_{N2}(z)$ are the noise errors referring to the input of the filters themselves. The signal transfer function, $STF(z)$, the noise transfer function $NTF_S(z)$ and $NTF_D(z)$ (associated with $E_S(z)$ and with $E_D(z)$, respectively), are equal to unity. Regardless of whether the EF or CIFF filter option is used, note how, since $NTF_D(z) = 1$, the mismatch error is not shaped. Now, if a block L(z) is added, the noise transfer function referring to the mismatch error $E_D(z)$ would be described by Equation (19). If that block has a high-pass function, $(1 - z^{-1})$, the mismatch error can be placed outside the BW. The challenge is the synthesis of circuits for L(z), which should be added to the system to model this filter. This idea has already been applied to a ΔΣ modulator [51].

$$NTF_D(z) = \frac{D_{out}(z)}{E_D(z)}, \tag{19}$$

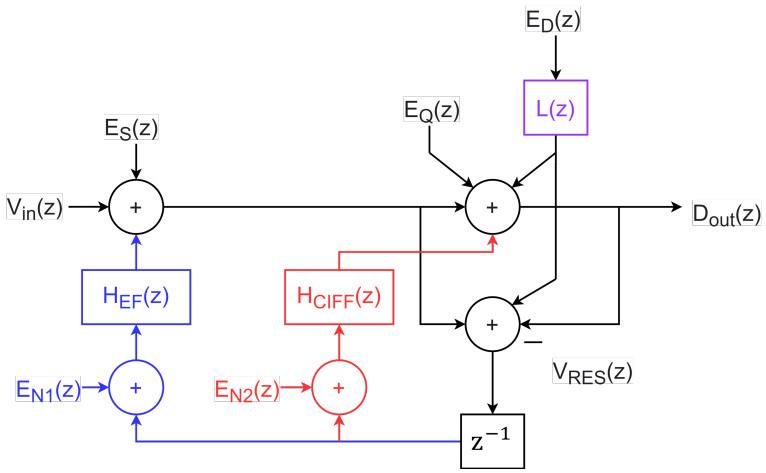

Figure 27. Block diagram of a NS SAR with the different error sources. The block L(z) that is added to the error, E_D(z), is intended to perform a noise shaping.

3.3. CDAC Mismatch Correction, an Alternative: NS DEM

kT/C noise is another problem where the efforts to obtain better metrics are focused. During the sampling process, thermal noise with a total power of kT/C "sneaks" into the sampled signal. Solutions include the design of an input buffer [52] (to alleviate the load on the input source), increasing the value of the unit capacitors, active cancellation [53], and also improvements in the design of the CMOS switch with bootstrapping [54] and clock boosting [55] techniques. The noise in the comparator is another problem of interest, because it can be a limiting factor in the resolution of the quantizer. Tri-Level Voting schemes have been applied to reduce noise. This technique is preferred over Majority Voting [24] because it takes advantage of more information in the comparator output data and provides an additional decision level, and because in the last two conversion cycles (corresponding to the LSB), it will repeatedly activate the comparator four times for each bit, then the result will be determined. By doing so, the comparator noise must be suppressed through averaging [19].

Another technique for noise reduction in the comparator is the appropriate selection of the comparator architecture (such as a chopped transconductor), where switches are incorporated to generate a square wave modulator, also known as chopping modulation [56], in such a way to shift the low-frequency spectrum out of the BW. The offset is amplified, passes through the modulator, and is removed by a low-pass filter. The disadvantage of this technique is that the added square signal has to be exactly 50% duty cycle, so that it does not provide a residual DC signal; glitches are also generated by the effect of charge injection and coupling of clock systems. A NS SAR has been used in the input buffer and in the IIR filter [20].

4. Trends on Dynamic Comparison

4.1. CMOS Comparators

Comparators are an essential block in many mixed-signal circuits, especially in the analog-to-digital converter (ADC). In an ADC, the comparator plays an important role, serving as the conversion bridge between the physical and digital worlds. The performance in low-power ADCs, such as successive–approximation–register (SAR) ADCs, strongly depends on the comparator's performance. This includes characteristics such as noise, offset, common-mode voltage, influence accuracy, and resolution, while the comparison speed determines the sampling rate of an ADC [57]. Typically, between 40% and 60% of the power consumption in a SAR ADC is due to the comparator [58–61]. With the development of manufacturing processes and the trend towards decreasing supply voltage, strict requirements are imposed on quantization noise, making energy consumption reduction a challenge, assuming that comparators are not scalable unlike digital blocks in a SAR ADC. The comparator, as a fundamental part in power contribution, must have sufficient gain to reduce input-referred noise (IRN), be insensitive to common-mode voltage (V_{CM}) and PVT variations, as well as have low power consumption.

The comparator, as it was originally understood, has evolved and its design is becoming more complex every day because it now must perform more tasks. Figure 4b shows the conventional two-stage, continuous-time comparator, which is based on an uncompensated Miller topology. Although one of its drawbacks is the offset, properly dimensioning the output stage, and specifically the M_{2pc} transistor, it is possible to reduce the offset to acceptable values; in this proposal all transistors operate in strong inversion. However, for low-power applications it is unsuitable because of its static dissipation. Currently the complexity in designing a comparator can be reduced a little by defining its application, that is, by establishing the bandwidth of the signal and the resolution of the converter of which it is part. In other words, the comparator is custom designed, which means that the necessary technology is available for its implementation. One option to reduce power consumption is the CMOS 3.3 V simple-switched amplifier. Figure 5b shows the two- and three-stage design, where C_1–C_2 are parasitic capacitances and the M_{1a} and M_{1b} transistors are responsible for making the voltage comparison. Note that the V_{GS} voltage of M_{1b} is

formed by the voltages to be compared. For illustrative purposes consider the two-stage comparator, marked with the shaded area. First, assume that the initial value of V_{in-} is V_{DD} and RST is high, therefore M_{1b} is switched off. In this condition C_1 is precharged to V_{DD} and C_2 is discharged to 0 V. When V_{in-} varies from V_{DD} to 0 V, there is a time t_0 in which M_{2a} turns on and C_1 discharges. That voltage is amplified by $M_{2a} - M_{2b}$, which is an inverter amplifier. To restore the phase, another $M_{3a} - M_{3b}$ amplifier is used, which apparently favors the rapid response of the comparator. Let us suppose the output V_o should have a large swing, from 0 to 3.3 V, as the input changes $\pm$1.0 mV. So, the required gain is just 3.3 V/2 mV = 1650 $\equiv$ 64.35 dB [62]. However, this proposal is not suitable for low-voltage and low-power consumption because noise affects the converter's resolution.

As we know, electronic noise, offset, mismatch, power consumption, sampling rate, and non-linearity of network elements, to name a few unwanted effects, affect the precision of the conversion in different proportions, that is, it is very important to know which are the most relevant sources of error and focus the greatest effort there. Nowadays, using comparators based on the operation of a latch is common practice. On the one hand, power consumption benefits, now being a dynamic consumption. This characteristic, on the other hand, causes the comparator to perform an amplification task and then another of comparison. Although the tasks are defined in each clock cycle, the aim is to optimize energy efficiency in each comparison, so that energy consumption is efficient in each conversion step. Therefore, as the trend in SAR ADCs is low power consumption, dynamic comparators are the best option.

A dynamic comparator shown in Figure 6c (without transistors M_{ref}) is an example of a latch-based comparator that is periodically regenerated. In this proposal the comparator also draws current from V_{DD} only when the state changes. This way, the energy needed to change the state is as small as in a digital gate. In practice this comparator would provide a large output swing that is well suited for the digital processing following the comparator. Now, the basic operation can be described in three phases. First, do not consider the transistors M_{n4b} and M_{n4c}, and assume that $clk = 0$. In this phase the capacitors $C_X - C_Y$ and $C_P - C_Q$ are precharged to V_{DD} and V_{in}, respectively, and while M_{n3a} and M_{n3c} are on M_{n2a} and M_{n2c} are off. In the second phase $clk = 1$ the capacitances $C_X - C_Y$ and $C_P - C_Q$ begin their discharge. That voltage ΔV_{in} in C_P and C_Q flows as the current to V_{out+} and V_{in-}, respectively. In the third phase the signal through M_{n2a}/M_{n2c} and with the load M_{n1b}/M_{n1c} is amplified with a factor corresponding to a cascode inverter amplifier, causing V_{out+} to ground and V_{out-} to V_{DD}. It can be verified that if the current extracted from each capacitance (ΔI_{CM}) is constant, the approximate gain is:

$$|V_{out+} - V_{out-}| \approx g_{m,n} \Delta r_{out} |V_{in+} - V_{in-}|, \tag{20}$$

where Δr_{out} is the output impedance and $\Delta I_{CM} = C_P$, $Q \Delta V_{in}/\Delta t$ with C_P,$Q = C_P = C_Q$; Δt is the time the amplification lasts. It is important to say that the input transistors (M_{in}) operate in the triode region, which is relevant because when the latch is regenerated ($clk = 1$) the currents of both M_{sw} transistors are steered so that the logical state of V_o is established. However, the mismatch in resistance associated with M_{in} transistors affects the expected state, causing a slow response. One solution is to reduce both the equivalent resistance and mismatch by including the M_{ref} transistors, also operating on triode and where V_{ref+} and V_{ref-} are bias voltages. In this proposal the input voltage that causes both resistors to be equivalent is the threshold voltage of the comparator [55]:

$$(V_{in+} - V_{in-})_{threshold} = \frac{W_{ref}}{W_{in}} (V_{ref+} - V_{ref-}), \tag{21}$$

the one that can be adequately proposed by the designer. However, the noise generated by the comparator is inversely proportional to the efficiency, g_m/I_{CM}, and to minimize this undesirable effect, a higher value of gm or equivalently greater gain is required (see Equation (22)). But, because the bias current is strongly related to the voltage of V_{CM} and

the common-mode input efficiency is compromised. Consequently, one solution is to have independent control of both the latch and amplifier function.

$$\sigma_n^2 \propto \frac{4kT}{\frac{g_m}{I_{CM}} V_{th,n} C_x}, \tag{22}$$

4.2. StrongARM Latch

Within the state of the art, one of the most used comparators in recent years is the StrongARM Latch (SA) [63]. Its popularity stems from being the first single-stage latch-type comparator (the pre-amplification stage and latch are in a single block), not consuming static power, producing rail-to-rail outputs, and having input-referred noise (IRN) dependent on the input differential pair. However, because it lacks isolation between the latch block and the differential input, the SA latch exhibits kickback noise, which hampers performance and energy efficiency [63]. The classic SA latch is depicted in Figure 28.

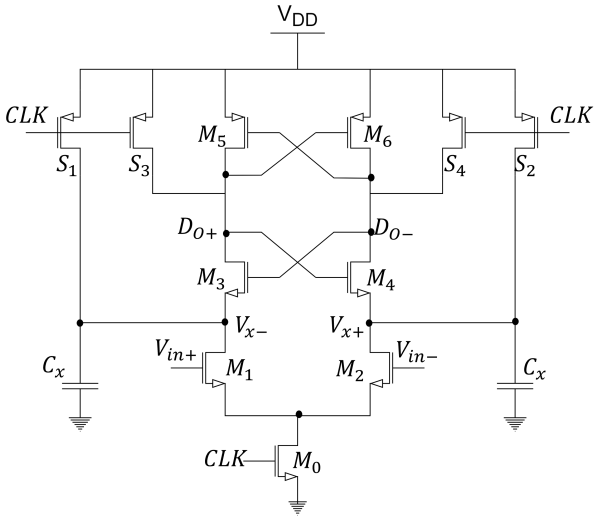

Figure 28. StrongArm Latch.

It can be observed that transistors M_1/M_2 and M_0 implement the pre-amplifier stage, while the two cross-coupled pairs M_3/M_4 and M_5/M_6 and the four switches S_1–S_4 implement the latch stage. Its operation can be summarized in two phases, the reset phase and the amplification phase. In the reset phase, when CLK = 0 (low state), transistors M_1 and M_2 are turned off, and the transistors operating as switches S_1–S_4 are turned on, precharging nodes D_{o+}, D_{o-}, V_{x+}, V_{x-} with a value equal to V_{DD}. When CLK = 1 (high state), S_1–S_4 are turned off, and M_1 and M_2 are turned on, allowing a differential current proportional to $(V_{in+} - V_{in-})$ to flow from the capacitors C_x. Here, the amplification operation occurs in which the comparator provides gain and works as a dynamic integrator, where the input signal is continuously integrated by the capacitor C_x. The amplification phase has an approximate time represented by:

$$T_{int} \approx (\frac{C_x}{I_{CM}}) V_{THN} \tag{23}$$

where I_{CM} is the common-mode current and V_{THN} is the threshold voltage of the NMOS transistors. The voltage gain is represented by:

$$A_v \approx (\frac{g_{m1,2}}{C_x}) T_{int} \approx (\frac{g_{m1,2}}{I_{CM}}) V_{THN} \tag{24}$$

where it is observed that the gain depends on the efficiency of g_m/I_D of M_1/M_2 and V_{THN}. The voltage at nodes V_{x+}, V_{x-} decreases to a value of $V_{DD} - V_{THN}$, and then transistors M_3/M_4 are turned on and allow the current to flow from output nodes D_{o+} and D_{o-},

where the potential of these nodes reaches a value of $V_{DD} - V_{THP}$ at which point transistors M_5/M_6 are turned on. The positive feedback from these transistors eventually leads one of the outputs to return to V_{DD}, while the other drops to GND. The comparator noise is represented by:

$$\sigma_n^2 \approx \left(\frac{I_{CM}}{g_{m1,2}}\right)\frac{4kT\gamma}{V_{THN}C_x} \tag{25}$$

where it can be observed that to reduce thermal noise, a high value of g_m/I_{CM} is needed, as well as a large value of C_x. It is observed that to design a low-noise comparator, it is necessary to have a large-gain A_v. There are certain disadvantages, such as the limitation of low voltage, energy waste due to the total discharge of C_x, the voltage gain is limited by the value of V_{THN}, and because transistor M_0 is biased in the weak inversion region, the current I_D is strongly correlated with the common-mode input voltage (V_{CM}), making the comparator performance susceptible to variations in V_{CM}.

4.3. Double-Tail Comparator

The double-tail comparator presented in [64] is shown in Figure 29. This comparator avoids the kickback issue by separating the pre-amplifier stage $(M_1 - M_5)$ from the latch stage $(M_6 - M_{12})$. It features independent control of the common-mode current I_{CM} for both the pre-amplifier and the latch, achieved through the addition of separate tail transistors (M_3/M_{12}), resulting in a shorter delay in the output response. During the reset phase (CLK = 0), M_3 and M_{12} are turned off. Transistors M_4/M_5 pre charge nodes V_{x+} and V_{x-} to V_{DD}, causing transistors M_6/M_7 to discharge output nodes D_{o+} and D_{o-} to GND. During the amplification phase (CLK = 1), M_3 and M_{12} are turned on, M_4/M_5 are turned off, and voltages at nodes V_{x+} and V_{x-} gradually discharge to GND. During the reset phase, these nodes must be charged from ground to V_{DD}, resulting in an energy consumption equal to $2C_xV_{DD}$. A drawback of the double-tail comparator is that latch transistors M_6/M_7 operate in the linear region, reducing the effective gain between stages, leading to increased noise and offset [59]. Using this same structure, Babayan et al. [65] performed a delay analysis for dynamic comparators and proposed a new version of the double-tail comparator with low-voltage and low-power characteristics. The main idea is to increase the output voltage variation $\Delta V_{x+}/V_{x-}$ to reduce delay. For this purpose, two control transistors are added in parallel with M_4/M_5 cross-coupled.

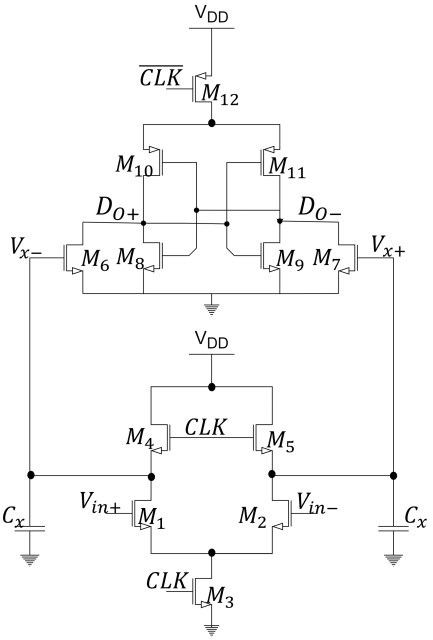

Figure 29. Double Tail Comparator.

4.4. Dynamic Two-Stage Comparator

On the other hand, the architecture of the dynamic two-stage comparator [59] shown in Figure 30a features a separation between the input blocks, comprising the amplification stage (M_0–M_5) with an input differential pair (M_1/M_2) and the second stage (M_6–M_{13}) which includes a simple voltage amplifier (M_5/M_6) and a positive feedback amplifier to achieve rail-to-rail digital output. This comparator operates in two phases, reset and amplification. The reset stage occurs when CLK = 0, where the capacitors C_x connected to nodes V_{x+}/V_{x-} are charged to V_{DD}, and the outputs D_{o+}/D_{o-} fall to GND. When CLK = 1, the amplification phase occurs. The differential output voltage $V_{x+} - V_{x-}$ increases, while the common-mode voltage output V_{CMO} decreases to GND. As V_{CMO} approaches the threshold voltage V_{THP} of the PMOS transistor, the input differential pair of the second stage starts amplifying, thus, while the differential output of the second stage increases, positive feedback ensures rail-to-rail outputs. Power dissipation in the first stage stops when C_x has discharged completely. Power dissipation in the second stage stops when the positive feedback amplifier has settled. When the clock signal CLK returns to low, all nodes (V_{x+}/V_{x-},D_{o+}/D_{o-}) are pre-charged to their original values. Therefore, this comparator virtually has no energy dissipation when the comparator is inactive. The first stage of the comparator improves the energy efficiency of the system because it is considered to operate in the weak inversion region. This gain significantly reduces the input noise of the second stage. On the other hand, the capacitors connected to the output nodes V_{x+}/V_{x-} are fully discharged, which still implies evident energy consumption in each comparison process.

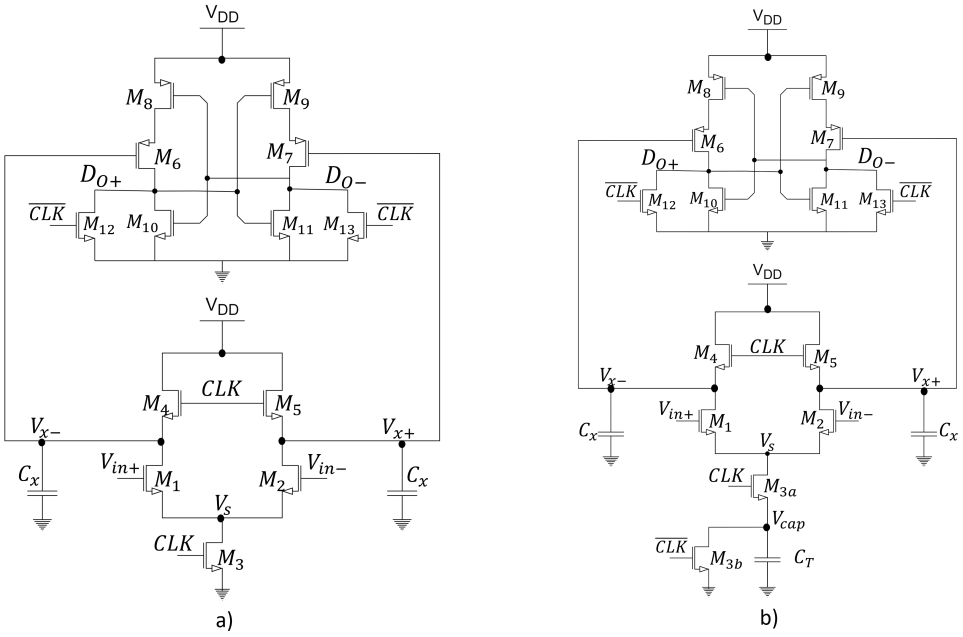

Figure 30. (**a**) Dynamic two-stage comparator and (**b**) dynamic bias comparator.

4.5. Dynamic Bias Comparator

The architecture of the dynamic bias comparator is presented in [66]. The architecture is shown in Figure 30b and is similar to Figure 30a, with the exception that the transistor M_3 is replaced by a transistor M_{3a}, a tail capacitor C_T, and a transistor M_{3b}. The idea of this architecture, in addition to reducing energy consumption, is to obtain an increase in the gain factor. The topology includes capacitors (C_x and C_T) that perform two functions. On the one hand, they are useful to control charge and discharge, and on the other hand, they minimize the effect of thermal noise. It should be noted that the M_1/M_2 transistors operate in weak inversion, so the current is very small and thus increases the gain. This proposal not only increases the g_m/I_{CM} efficiency but also the input referred noise (IRN)

is now inversely proportional to C_x, (see Equation (26)). In other words, C_x now does not represent a parasitic capacitance but rather a capacitor that is selected for a particular gain and a desired SNR [66]. One drawback of this architecture is that it exhibits higher delay compared to the SA latch [64]. Another inconvenience arises in corner process analysis or in large common-mode input voltage variations, causing the integration phase to become unstable.

$$\sigma_n^2 \propto \frac{2kT}{\frac{g_m}{I_{CM}}\Delta V_d C_x}, \tag{26}$$

4.6. FIA-Based Comparator

The Floating Inverter Amplifier-based comparator is proposed in [67], comprising a pre-amplifier floating inverter amplifier (FIA) and a SA latch. The architecture can be seen in Figure 31. It is robust against corner process variations and common-mode input voltage fluctuations. It utilizes a reserve capacitor C_{RES}, which is charged during the reset phase to a value of V_{DD} and serves as a power source during the integration phase. It also optimizes energy efficiency and is resilient to PVT variations. It is an architecture that provides isolated voltage to the amplifier (M_1–M_4). The input and output currents of C_{RES} must be equal ($I_{AMP+} = I_{AMP-}$), yielding a common-mode current $I_{X,CM} = 0$, hence achieving a constant output common-mode voltage without a CMFB circuit. This is an important point, maintaining a constant output common-mode voltage, as it can limit the accuracy of the comparator and consequently the resolution of the ADC.

The transconductance is expressed as:

$$g_m(t) \approx \frac{2I_D(t)}{nU_T} = \frac{I_{AM}(t)}{nU_T} \tag{27}$$

where $I_D(t) \approx 1/2\ I_{AM}(t)$ is the instantaneous current of the transistor with a small differential input voltage, n is the slope factor in weak inversion, and $U_T = kT/q$ is the thermal voltage. The differential output voltage can be approximated as:

$$\Delta V_{x,DM}(t) \approx \frac{\Delta V_{in,DM} \int_0^t I_{AMP}(\tau)\, d\tau}{nU_T C_x} \tag{28}$$

The source voltage V_{RES+}/V_{RES-}, and the change $\Delta V_{RES}(t)$ is obtained as follows:

$$\Delta V_{RES}(t) = nU_T In\left(1 + \frac{I_{AMP}(0^+)}{2nU_T C_{RES}} t\right) \tag{29}$$

The integration gain is calculated as:

$$A_v(T_{int}) = \frac{2C_{RES}\Delta V_{RES}(T_{int})}{nC_x U_T} \tag{30}$$

The IRN of the FIA at the end of the integration time can be calculated as:

$$\sigma_n^2(T_{int}) = \frac{2nkT}{C_{RES}\Delta V_{RES}(T_{int})}\frac{I_D}{g_m} \tag{31}$$

As can be observed, the IRN is inversely proportional to g_m/I_D, demonstrating that with higher gain, the noise effect decreases. It is also observed that using a large C_{RES}, as well as large changes in $\Delta V_{RES}(T_{int})$, increases the gain. Therefore, with the FIA serving as the pre-amplification stage, it provides sufficient gain to reduce IRN. However, this topology exhibits a limited response speed [67,68]. To address this speed limit, a modification to the FIA-SA is performed in [68], enhancing both gain and response speed while preserving the advantages of the FIA pre-amplifier, achieved through the utilization of a latch-embedding

floating amplifier (LEFA). In [68], a design approach is described to achieve higher gain in the first stage by placing the input pair in a parallel latch configuration. This configuration allows for positive feedback resulting in greater gain and faster decision-making.

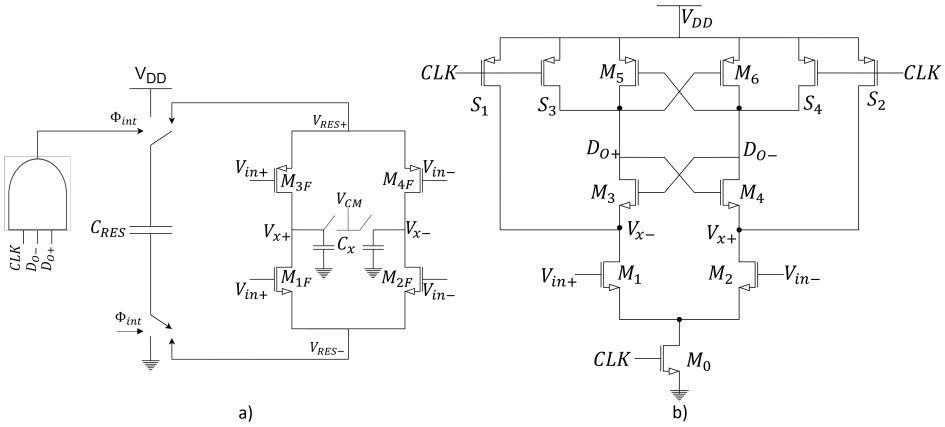

Figure 31. (**a**) Floating inverter amplifier and (**b**) SA latch.

4.7. Low-Power Comparator

In [58], a modification to the dynamic two-stage comparator is proposed, adding a cross-coupling mechanism around the input differential pair, which prevents the complete discharge of the comparator's internal nodes when small differential signals are present at the input, thus reducing energy consumption per comparison. It is worth noting that this architecture does not use additional capacitors like the FIA-SA [67] or the DB [66].

As observed in Figure 32, the pre-amplification stage features two transistors with cross-coupling (M_8 and M_9) and two additional transistors acting as switches (M_6 and M_7). During the reset phase, the pre-charge transistors (M_4, M_5, M_6, and M_7) drive the V_{x-}, V_{x+}, N_1, and P_1 nodes to V_{DD}, while transistors M_{16} and M_{17} reset the output nodes of the regenerative latch (D_{o+} and D_{o-}). With M_3 turned off, the current flow from V_{DD} to GND is cut off.

The amplification phase consists of two sub-phases. In the first sub-phase, the gates of M_3 and M_8 are connected to V_{DD}, causing node N_1 to discharge rapidly due to the drop in IR across the switches (M_3 and M_8). Node P_1 behaves similarly. Transistors M_1 and M_2 start conducting current flow, and M_8 and M_9 operate in the linear region. This causes the voltage at the intP and intN nodes to decrease, and the voltage at N_1 and P_1 to increase slowly, resulting in changes in the differential input pair's V_{GS} voltage, reducing transconductance g_m. This behavior may increase the conversion time for small differential input voltages. In the second sub-phase, the circuit changes its behavior as the V_{x+} node becomes static. This results in a reduced discharge speed of the V_{x-} node. The operational timing behavior ensures that V_{x+} and V_{x-} are only discharged to specific voltages below V_{DD}, improving energy efficiency compared to conventional architectures.

This architecture achieves higher energy efficiency without additional capacitors or complex logic, based on a simple cross-coupling mechanism around the differential input pair. However, this approach results in a slight increase in noise.

In general, it can be concluded that one of the trends in the design of the comparator is to prevent the capacitances in the output nodes from being completely discharged. This property minimizes energy consumption, increases the gain, and reduces the effect of thermal noise. Consequently, the proposed topologies experience an increase in the number of transistors, and capacitors are even manufactured to improve the performance of the comparator and the systems in general. Some proposals do not include capacitors but add more transistors that operate as switches. Cross couplings and separation of functions are other characteristics of comparators that increase the complexity of behavioral analysis as well as analytical analysis to quantify various figures of merit. However, models of design

have been obtained that not only depend on parameters that are under the control of the designer, but also on some fundamental technological parameters. But, nothing has been said about the temperature T, this being a parameter that directly affects the generation of thermal noise. It is not the subject of this contribution to incorporate the analysis of the comparator in the face of temperature variations, including evaluating the performance of the system at cryogenic temperatures. But, much in the design of A/D conversion circuits still remains to be said.

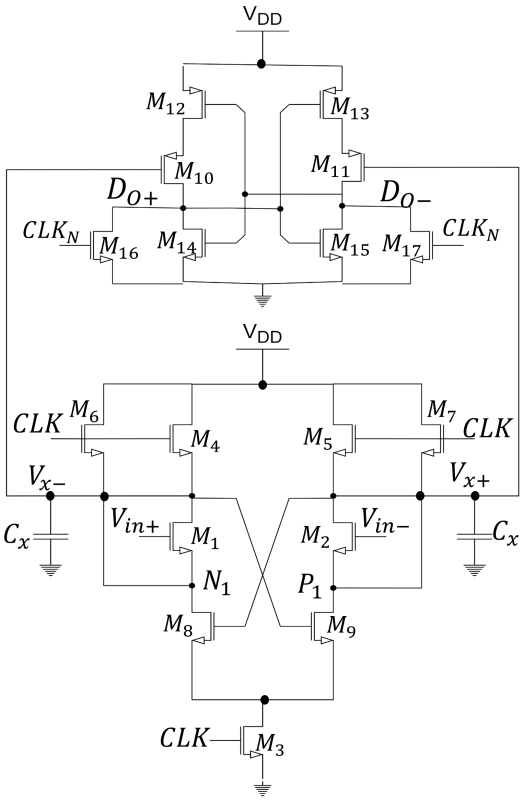

Figure 32. Low-power dynamic comparator.

5. Trends, Further Advances, and Conclusions

It is a fact that for certain critical applications, NS SAR can be considered as a natural substitute for conventional discrete time ΔΣ modulators [12]. However, despite its great low power consumption characteristic, for mainly applications, a wider BW and higher resolution are required. For this reason, it has also been opted for approaches where architecture hybridizations are carried out, and without a doubt in the future there will be implementations with higher BW, low power consumption, and devices that exceed the 100 dB SNR barrier. From the latter, solutions have been developed to increase the sampling frequency without losing BW. The idea is to have more than one ADC, and operate multiple connection channels and overlap their conversions [69]. Another idea is to use the NS SAR as a quantizer in a continuous-time SD modulator [70] and improve the overall performance of the ADC. Undoubtedly, the idea to achieve higher order NTFs that has recently reported more guidelines and contributions, it is NS SAR Multi-stage noise-shaping (MASH) architectures. Figure 33 shows the schematic of a MASH 2-2 without OTA [71] based on an EF structure, it has achieved a fourth-order NTF at 500 kHz BW. Similarly, other interesting works on MASH have been reported [72,73]. Incremental NS SAR implementations should not be neglected either, as they may be promising architectures in the near future [74,75].

It is also interesting how the use of buffers has become indispensable in the circuit design and how Dynamic Level Shifting has been used in a subrange NS SAR [52] to adjust the output of the buffer, in addition to applying a correction to the so-called Inter-Symbol

Interference (ISI) which also causes CDAC mismatch. This correction technique is proposed to further improve linearity. However, it must be considered that the comparator in a SAR A/D consumes a high percentage of energy. And, if it is also considered that the development of manufacturing processes tends to reduce the power supply, the designer must not only propose appropriate conversion architectures, but also design active blocks with minimum energy consumption. The best example is the comparator, whose performance has been improved with the development of technology. As an example, today's comparators, compared to the pioneer two-stage, have reduced energy consumption by approximately 86%. But, not everything has been said. Energy savings possibly lie in reducing, in a controlled manner, the operating temperature, for example, why not a few degrees Kelvin.

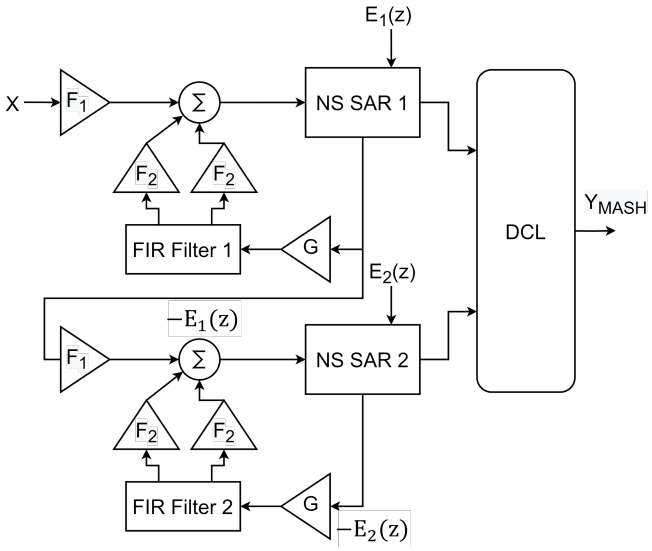

Figure 33. NS SAR MASH 2-2 fourth-order without OTA [71].

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